The Design and Implementation of Gated Service Polling System Based on FPGA

Longjun Liu, Hongwei Ding, Qianlin Liu, Liyong Bao, Zhijun Yang, and Xiuying Lu

***Abstract*—The polling control strategy is a kind theory of important resource allocation scheduling. Because of its equity, flexibility, efficiency and practicality, etc, it has been widely used in industrial process control, traffic control, communication network, and so on. This paper presents a design and implementation of gated service polling system based on FPGA. The system makes full use of the reconfigurable and flexible of FPGA. The method of combining the hardware description language Verilog HDL and the principle diagram is used for the design. The correctness of the system designed is verified by simulation test and statistical analysis.**

***Index Terms*—FPGA, gated service, polling system, polling cycle, queue captain, wireless sensor network.**

I. Introduction

In recent years, because of the rapid development of technologies like wireless communication, integrated circuits, sensors and micro-electromechanical systems (MEMS), the mass production and use of wireless sensors which is low-cost, low power and multi-functional has been promoted [1]. A large number of wireless sensors are distributed in the target area as network nodes, they form a multi-hop and self-organizing network system through wireless communication, namely wireless sensor network. The sensors in the network sense collect and process the information of the objects in the target area by cooperative sensing and send them to the observer [2], [3]. By analyzing the received data, users can make the sensor network do the configuration management and task delivery.

As the wireless sensor network low cost, high reliability, easy management and other excellent features, its application is very wide. Ref. [4]-[6] respectively study the application of wireless sensor networks in modern military, environmental monitoring, digital agriculture, industrial production [7], medical care [8], intelligent transportation [9]. In the wireless sensor network, the MAC protocol plays an important role. It determines how to use the wireless channels, it also allocates the communication resources reasonably for the nodes, effectively avoid multiple nodes using the channel at the same time. The MAC protocol ling in the bottom is one of the key network protocols to ensure efficient wireless sensor network's communication, it determines the channel utilization, network delay, energy consumption and plays an important role in network performance. The characteristics, advantages and disadvantages of existing MAC protocols in wireless sensor networks are analyzed in [10], [11]. Because of the unique characteristics of the polling system, the MAC protocol based on polling mechanism has become a research hot spot. The basic model of the polling system is the policy control model of the service station and queuing queues (terminals). The service station provides services for queues in the system according to polling mode [12].

FPGA chips with low power consumption, parallel computing power, good programmability and other characteristics are increasingly widespread in the field of communications. With the increasing integration, the development of communication systems can greatly improve the transmission efficiency, reduce network delay, enhance the anti-interference and have more flexible configurability [13]. The development of polling control system using FPGA can effectively improve the system delay and transmission efficiency, and possess the property of better reliability, re-al-time and scalability.

II. System Model

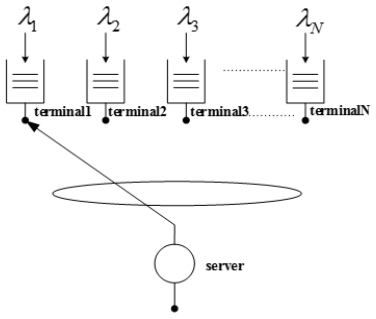

Fig. 1. The basic model of the polling system.

The basic model of the polling system [14] consists of 1 server and N terminals. According to the polling rules, the server serves each terminal service in turn in one direction, it services the last terminal and then returns to the first terminal, the basic system model is shown in Fig. 1 Polling system service strategy mainly have three kinds, namely the limited K = 1 service strategy, threshold service strategy and full service strategy. The polling system service rule adopting the threshold service strategy is that when the server polls the terminal for service, if there is no information packet to be transmitted, it'll be switched over to the next terminal after a conversion time, namely γ. And if there is an information

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packet to be transmitted, all of them will be transmitted, the information packet arriving at the terminal in the service process needs to wait for the next polling cycle to be transmitted. The working mode of the polling system can be described as three basic processes: the arrival process of the information packet (the arrival rate is λ), the process of the terminal receiving the service (the service time of a single packet is β), the conversion process between the terminals (conversion time γ) [15]. System service intensity is ρ ($N=\lambda\beta$), the system is stable when $\rho<1$.

Parameter the random variable $\xi_i(n)$ is the number of the information packets stored in the memory of the i terminal station at a specific time noted t_n. The state of the queuing system at time t_n can be expressed as $[\xi_1(n) \quad \xi_2(n) \quad \ldots \quad \xi_N(n)]$.

The probability function of the state variable can be expressed as

$$\begin{aligned} &G_i(Z_1Z_2\cdots Z_i\cdots Z_N) \\ &=\sum_{x_1=1}^{\infty}\cdots\sum_{x_N=1}^{\infty}\pi_i(x_1\cdots x_i\cdots x_N)Z_1^{x_1}\cdots Z_i^{x_i}\cdots Z_N^{x_N} \end{aligned} \tag{1}$$

$\pi_i(x_1\cdots x_i\cdots x_N)$ is the probability distribution function of the state variable. When the server turns to serve the $i+1$ terminal service at the moment t_{n+1}, there are relations as below:

$$\begin{cases} \xi_j(n+1)=\xi_j(n)+\eta_j(v_i)+\mu_j(u_i) \\ \xi_i(n+1)=\xi_i(n)+\eta_i(v_i) \end{cases} (j\neq i) \tag{2}$$

$$\begin{aligned} &G_{i+1}(z_1,z_2,\cdots,z_i\cdots,z_N)=\lim_{n\to\infty}E[\prod_{j=1}^{N}z_j^{\xi_j^{(n+1)}}] \\ &=\lim_{n\to\infty}E[\prod_{N}z_j^{\xi_j^n+\eta_j(v_i)}\cdot z_i^{\eta_i(v_i)}]E[\prod_{N}z_j^{\mu_j(u_i)}] \\ &=R_i[\prod_{j=1}^{N}A_j(z_j)]G_i[z_1,z_2,\cdots,z_{i-1},B_i(\prod_{j=1}^{N}A_j(z_j)),z_{i+1},\cdots,z_N] \end{aligned} \tag{3}$$

The expression $v_i(n)$ denotes the serve time for transmitting the information packet to the terminal No i, $u_i(n)$ denotes the polling conversion time for the server to switch from the No i terminal to the No $i+1$ terminal ,and $\mu_j(u_i)$ denotes the number of information packets entering the terminal No $j(j=1,2,\cdots,N)$ in the time marked $v_i(n)$. $A(z)$ denote the probabilistic function of the information packet arriving at processing random variable, $B(z)$ denotes the probabilistic function of the random variable for the service time, and $R(z)$ denotes the probabilistic function of the random variable for the polling transition time.

Defined $g_i(j)$ as the average queue length of the information packet in the terminal No j when the terminal No i is to receive services at the certain time t_n, then the formula for the average queue length of the threshold service system can be expressed

$$g_i(j)=\lim_{z_1\cdots z_i\cdots z_N\to 1}\frac{\partial G_i(z_1\cdots z_i\cdots z_N)}{\partial z_j} \tag{4}$$

$$g_i(i)=\frac{N\gamma\lambda}{1-N\rho} \tag{5}$$

Defined θ as the average time the server finishes serving all the terminals, that is, the polling cycle. Using the relationship between the polling period and the average queue length, we can conclude that:

$$\begin{aligned} \bar{\theta}&=\sum_{i=1}^{N}[g_i(i)\beta_i+g_i(i)\beta_i\lambda_i\beta_i+g_i(i)\beta_i(\lambda_i\beta_i)^2+\cdots+\beta_i\gamma_i] \\ &=N\beta_i g_i(i)\frac{1}{1-\rho}+N\beta_i\gamma_i \\ &=\frac{N\gamma}{1-N\rho} \end{aligned} \tag{6}$$

III. FPGA DESIGN AND IMPLEMENTATION

According to FPGA design flexibility, integration and top-down design ideas [16] ,to build the threshold service polling system, you need to design a module with the following specific functions: the source module to generate Possion distribution ,the terminal module to store information packet, the control module capable of controlling the server to polling services for each terminal in turn according to the threshold service strategy, and a receiving site module capable of receiving and reading the information packets of the corresponding terminal from the bus.

A. Source Module

Fig. 2. Source module block diagram.

It is very difficult to implement a Possion distribution with a specific arrival rate using the timing circuits on FPGA. In MATLAB, there is a Possion distribution function named poissrnd that directly generates a settable arrival rate. So, we use the poissrnd function in MATLAB to generate the Possion distribution, and use the ROM in the FPGA to read it, which can be assigned as the source module with Possion distribution characteristics. Fig. 2 shows the source block diagram. First of all, using MATLAB to generate possion distribution sequence, then using the ROM to read it, finally the module produce 8-bit source output information packet through the 8-bit mapping conversion.

B. Terminal Module

The terminal module should have the following functions: firstly, it can store the information packet arriving at the terminal when the write signal is valid; secondly, it can read the stored information packet according to the principle of FCFS (First Come First Served) when the read signal is valid; If the read signal is valid, but there is no packet in the memory, it'll go to the next terminal automatically. Terminal module circuit design is shown in Fig. 3. The four terminal memories are designed with four asynchronous FIFO, each of which operates under the control of the write signal, the read signal, and the write and read counters. Asynchronous FIFO output signal "empty" is the judgment signal indicating whether the terminal memory is empty. When the system accesses the terminal, if the signal named empty is high, it'll access the next terminal because it indicates the current terminal does not need to send information packets, otherwise, the terminal will be serviced. The write counter mainly performs the counting function of the information packets entering the terminal memory. When a terminal obtains service authorization, the write counter sends the current counter value to the read counter and reset itself to 0, then it starts sending the information packet in the terminal memory. Every time the terminal sends a message packet, the value of the read counter is decremented by one until it becomes to zero, and the module turns to the next terminal. This is consistent with the strategy for threshold service.

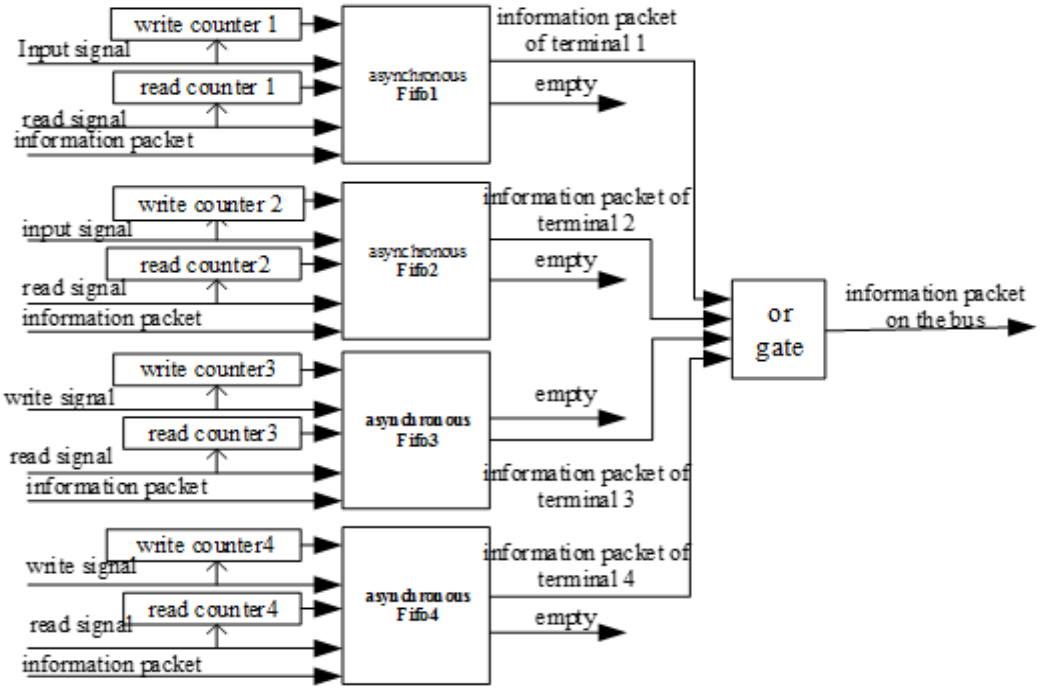

Fig. 3. 4 terminal circuit design structure.

C. Polling Control Module

Polling control module is assigned to complete polling services for the four terminals in accordance with the threshold service strategy. Fig. 4 shows the polling control module state transition diagram. Cr1, cr2, cr3, cr4 is the control signal deciding whether to continue to read controlled by the four read-out counters in the terminal module. If the value of the read counter is 0, the corresponding signal cr is low, otherwise it is high. If the current terminal read control signal c and continue to read control signal cr are high at the same time, the server continues to serve the terminal. If the read control signal cr is low, the next terminal is queried. This is consistent with the functionality that the polling control module has to perform.

D. Receiving Site Module

The receiving site module is to read the sending data correctly from the terminal corresponding to the site from the bus Fig. 5 is the receiving station circuit structure. The function of the filter module in the figure is to filter out incorrect all-zero information packets. After the receiving information packet is stored in the FIFO, FIFO read the information out under the condition of a sustained high-level read signal.

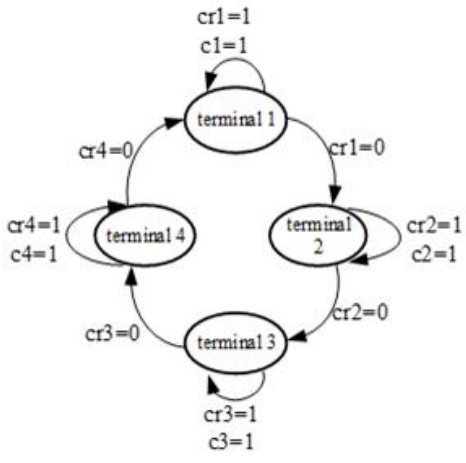

Fig. 4. Polling the control module state machine.

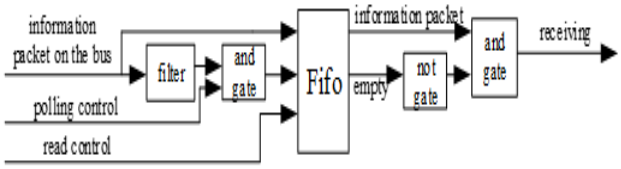

Fig. 5. Receiving site circuit.

E. System Implementation

Fig. 6 is a block diagram of the FPGA design of the gated service polling system. In the figure, the information packets generated by the four sources are stored and transmitted in the four terminals according to the threshold service rules under the control of the polling control module. The information packets sending by 4 terminals do "or" operation and sent to the bus. Since four terminals can't transmit information packets at the same time, there is no collision problem. Four receiving stations read the information packets sending from the corresponding terminal from the bus and complete the function of correct reception

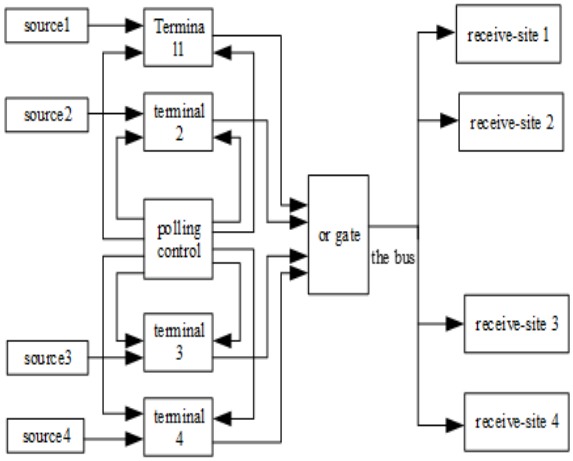

Fig. 6. Gated service polling system diagram of the FPGA design.

IV. Performance Evaluation

A. Simulation Test

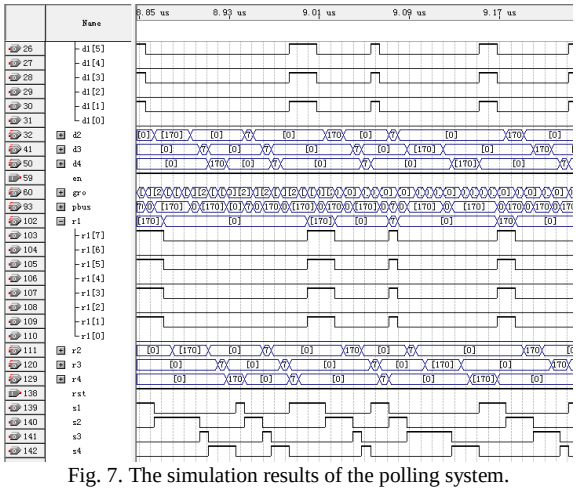

Fig. 7. The simulation results of the polling system.

Fig. 7 shows the simulation results of the gated service polling system. It can be seen that the information packet r1 received by the receiving station No. 1 is exactly the same as the information packet transmitted to the bus No 1 by the terminal No.1 except the time slot delay in time. The flag signals s1, s2, s3, s4 received by the four terminals are in accordance with the cyclic logic order from 1 to 4 to 1, which is in accordance with the requirements of the gated service polling system. In addition, it can be seen from the data transmitted on the bus named pubs, the utilization of the bus is relatively high.

B. Statistical Analysis

The total number of data packets and the number of cycles in the bus during the simulation process are counted. According to the threshold service strategy, we can get the statistical expression for the average queue length and the average polling cycle:

Average queue length

$$\tilde{g} = \frac{N_{gro}}{N \times N_{cp}} \tag{7}$$

Average polling period

$$\tilde{\theta} = \frac{T_{all}}{N_{cp}} \tag{8}$$

Among them, N_{gro} is the total number of information packets transmitted on the bus, N is the number of terminals, N_{cp} is the total number of cycles, T_{all} is the total simulation time. Table 1 shows the theoretical and statistical values of average queue length and average polling period under the condition of certain packet arrival rate λ=0.15, service time β=1, conversion time γ=2 but different simulation time, using (4), (5), (6), (7), (8) .

TABLE I: Statistical and Oretical Value

time target (us)	Theoretical queue length	statistical queue length	Theoretical polling period	Statistical polling period
T=100	1.5	1.37	10	9.33
T=200	1.5	1.39	10	9.48
T=400	1.5	1.41	10	9.57
T=600	1.5	1.43	10	9.64
T=800	1.5	1.46	10	9.76

It can be seen from Table I that the simulation statistic and the theoretical value are very close, and with the increase of the simulation time, the statistical value converges to the theoretical value, which is consistent with the theory.

V. Conclusion

Based on the working principle of the gated service polling system, this paper makes full use of the advantages of FPGA, such as high flexibility, strong computing power and on-the-spot programming, and combine the hardware description language Verilog HDL and schematic diagram to assign and implement the threshold service polling system from top to down. Through the simulation test and the statistical analysis, it is proved that the designed system has reached the requirement in the function and the index parameter, has realized the design goal. The MAC protocol based on polling mechanism designed by FPGA can effectively reduce transmission delay, avoid data collision and improve bus utilization. It has good application prospect in wireless sensor network and Ad Hoc network.

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